Code :RR321206 RR

III B.Tech II Semester(RR) Supplementary Examinations, April/May 2011
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. Implement the following gates with CMOS Logic and explain its working
   (a) Ex-OR gate.
   (b) 2 Input NOR gate.
2. Explain working principal of P-MOS transistor with sketches of its structure.
3. Explain clearly about different parasitic capacitances of an n-MOS transistor.
4. Design a layout for CMOS inverter.
5. Explain clearly the Job of the four types of simulators that are most commonly used for combinational logic design.
6. Draw the structure of carry select adder and explain its working principle.
7. Explain how power - down modes reduces the power consumption of the design.
8. Explain about switch - level simulation and give rules for evaluating switch - level simulation.

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